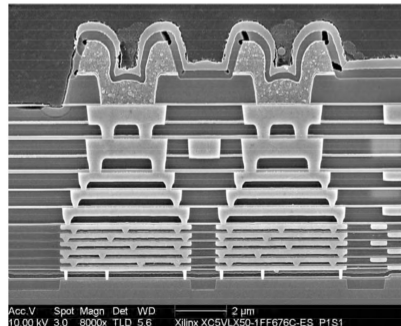


MEng VLSI - FPGA Introduction

Prof. Dr.-Ing. Friedrich Beckmann

Hochschule Augsburg

Figure 6:
Xilinx/UMC Virtex-5
UMC high-density
metal + low-k M1
- M6; mid-density
metals M7 - M9;
low-density M10 -
M11; Al M12.



Overview

Altera DE1 SoC Board

Cyclone V

Altera DE1 board

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Cyclone II

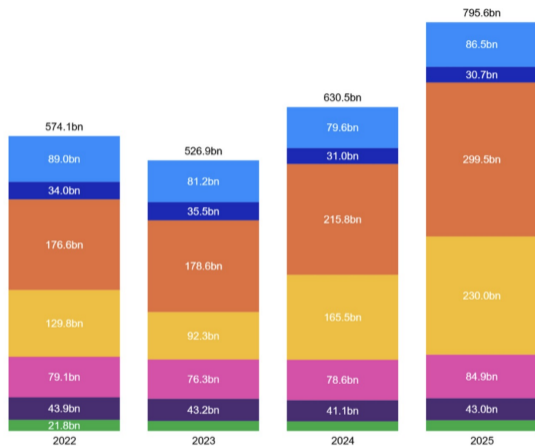
Cyclone V - more

Cyclone V HPS

Cyclone V FPGA

VLSI - Standard Cell
Design

Market Overview



YoY growth in percent

Segment Lv1	2022	2023	2024	2025
Analog	20.1%	-8.7%	-2.0%	8.7%
Discretes	12.0%	4.5%	-12.7%	-1.0%
Logic	14.0%	1.1%	20.8%	38.8%
Memory	-15.6%	-28.9%	79.3%	39.0%
Micro	-1.4%	-3.5%	3.0%	7.9%
Optoelectronics	1.2%	-1.6%	-4.8%	4.7%
Sensors & Actuators	13.7%	-9.4%	-4.1%	10.4%
Total	3.3%	-8.2%	19.7%	26.2%

- Analog
- Discretes
- Logic
- Memory
- Micro
- Optoelectronics
- Sensors & Actuators

FPGA World Market 2018: approx. 4.5 US\$ billion, i.e. 1% of total market
 Compare: Volkswagen 324 Billion Euros Sales in 2024

Source: https://www.wsts.org/esraCMS/extension/media/f/WST/7495/WSTS-Q4-Release-2025_-_06-Mar-2026.pdf

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Altera DE1 board

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Cyclone V FPGA

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Altera DE1-SOC Board with Intel Cyclone V 5CSEMA5F31C6N FPGA

Overview

Altera DE1 SoC Board

Cyclone V

Altera DE1 board

Tools

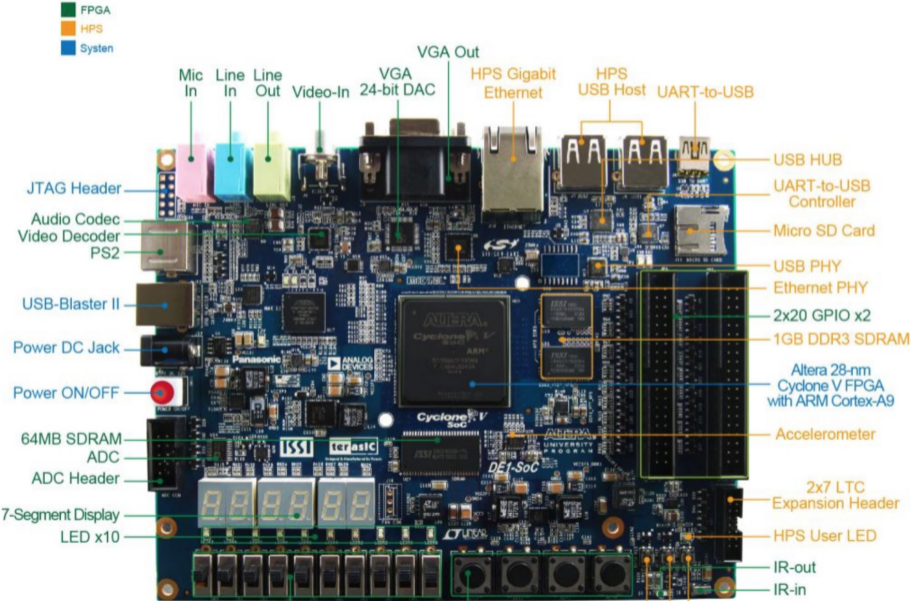
Cyclone II

Cyclone V - more

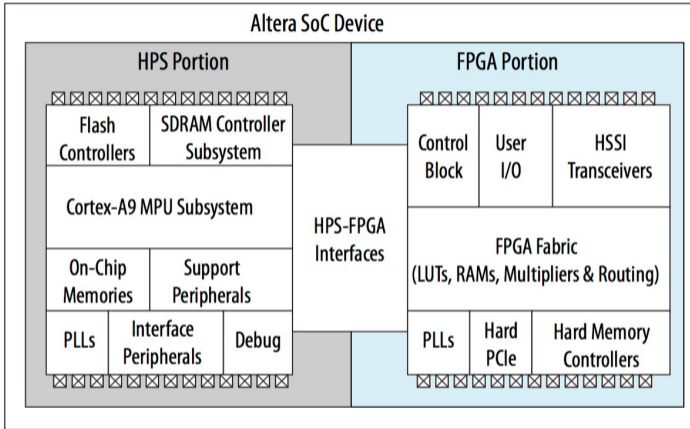
Cyclone V HPS

Cyclone V FPGA

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Intel Cyclone V SE - HPS / FPGA



SoC: System on Chip

HPS: Hard Processor System

FPGA: Field Programmable Gate Array

Source: Cyclone V Hard Processor System - Technical Reference Manual cv_5v4, 2018

Overview

Altera DE1 SoC Board

Cyclone V

Altera DE1 board

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Cyclone II

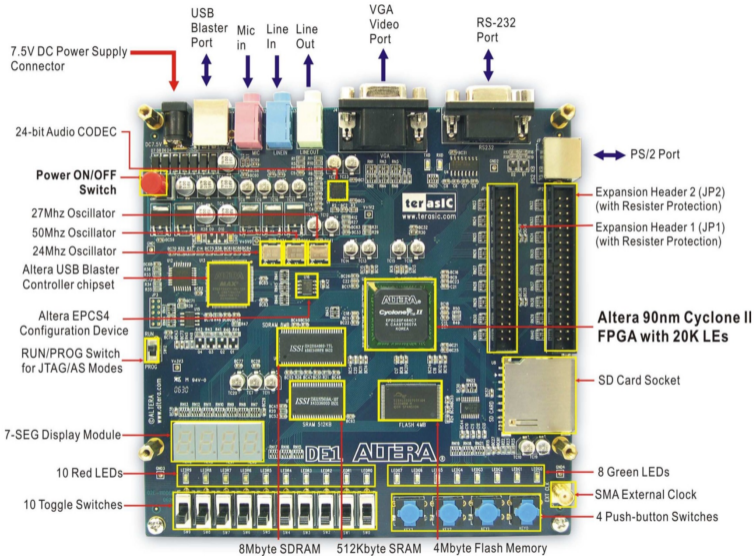
Cyclone V - more

Cyclone V HPS

Cyclone V FPGA

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Intel / Altera DE1 Board with Intel Cyclone II FPGA



Overview

Altera DE1 SoC Board

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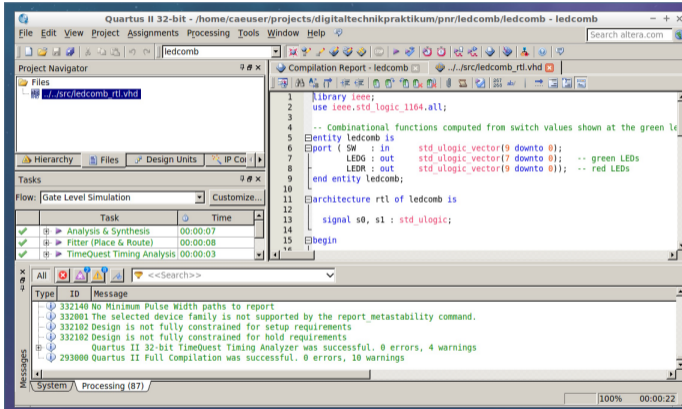
Cyclone V HPS

Cyclone V FPGA

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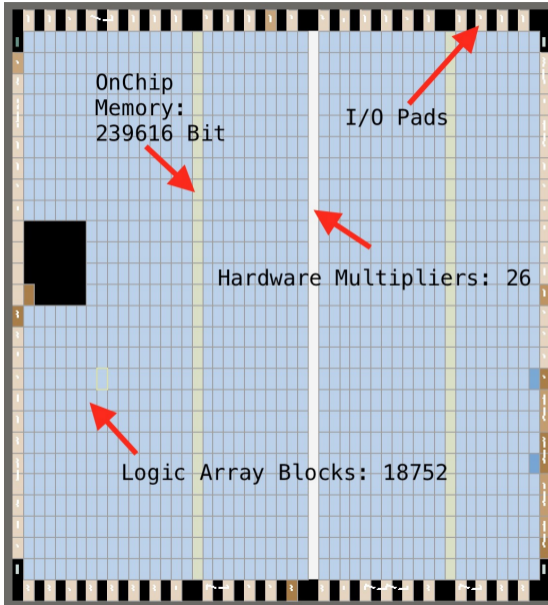
Software Tools and Board comparison



Intel/Altera Quartus 13 fpga synthesis software

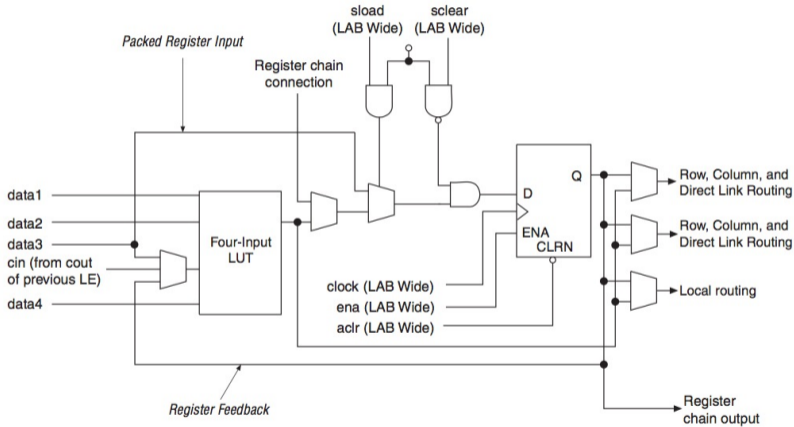
- ▶ Altera DE1 board
 - ▶ Intel/Altera Cyclone II FPGA
 - ▶ Quartus 13.0sp1 Software
 - ▶ Used in this course
- ▶ Altera DE1 SOC board
 - ▶ Intel/Altera Cyclone V FPGA
 - ▶ Quartus 18.1 software includes Processor

Cyclone II Floorplan



Cyclone II Logic Element - Normal Mode

Figure 2-3. LE in Normal Mode



Overview

Altera DE1 SoC Board

Cyclone V

Altera DE1 board

Tools

Cyclone II

Cyclone V - more

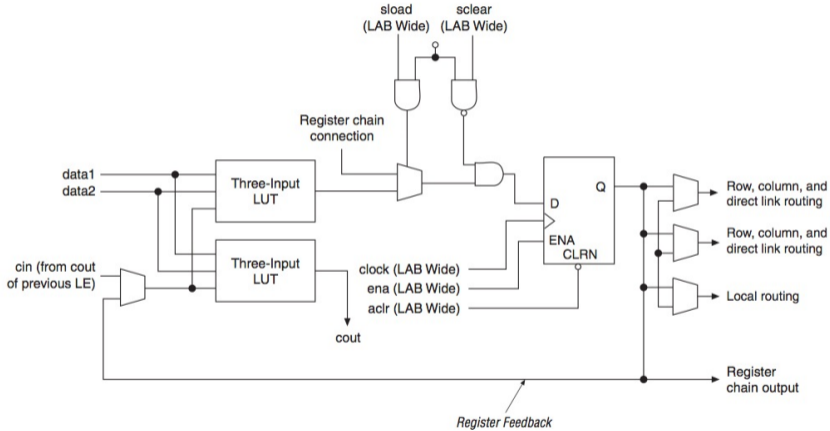
Cyclone V HPS

Cyclone V FPGA

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Cyclone II Logic Element - Arithmetic Mode

Figure 2-4. LE in Arithmetic Mode



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Altera DE1 SoC Board

Cyclone V

Altera DE1 board

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Cyclone V HPS

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Cyclone II Logic Element - Routing

Figure 2-5. Cyclone II LAB Structure

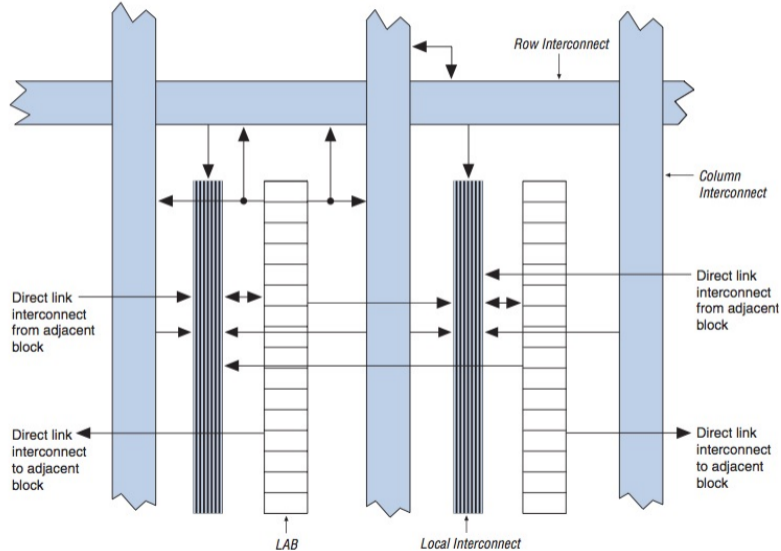
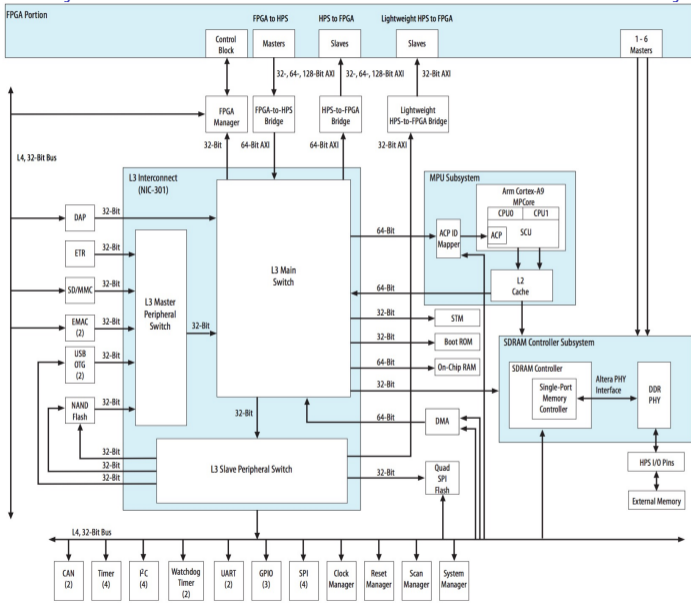


Table 1-1. Cyclone II FPGA Family Features			Altera DE1 Board			
Feature	EP2C5	EP2C8	EP2C20	EP2C35	EP2C50	EP2C70
LEs	4,608	8,256	18,752	33,216	50,528	68,416
M4K RAM blocks (4 Kbits plus 512 parity bits)	26	36	52	105	129	250
Total RAM bits	119,808	165,888	239,616	483,840	594,432	1,152,000
Embedded multipliers (1)	13	18	26	35	86	150
PLLs	2	2	4	4	4	4
Maximum user I/O pins	158	182	315	475	450	622

Source: Cyclone II Device Family Data Sheet

Intel Cyclone V SE - HPS - ARM Cortex A9 Processor System



Overview

Altera DE1 SoC Board

Cyclone V

Altera DE1 board

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Cyclone II

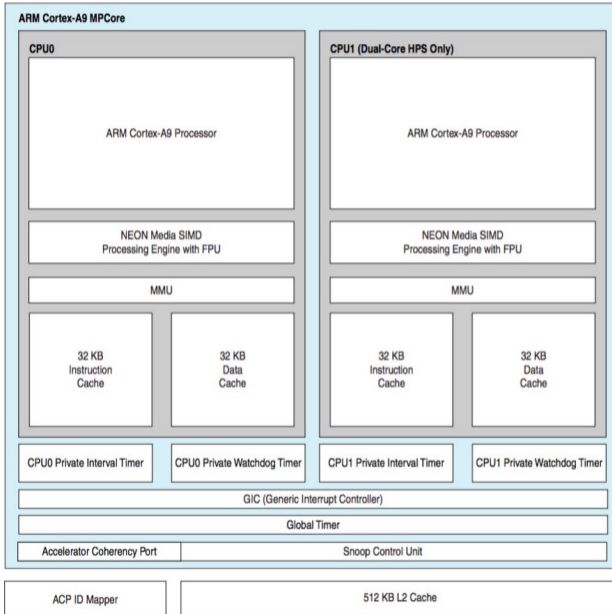
Cyclone V - more

Cyclone V HPS

Cyclone V FPGA

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ARM Cortex A9 Processor Subsystem



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[Altera DE1 SoC Board](#)

[Cyclone V](#)

[Altera DE1 board](#)

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[Cyclone II](#)

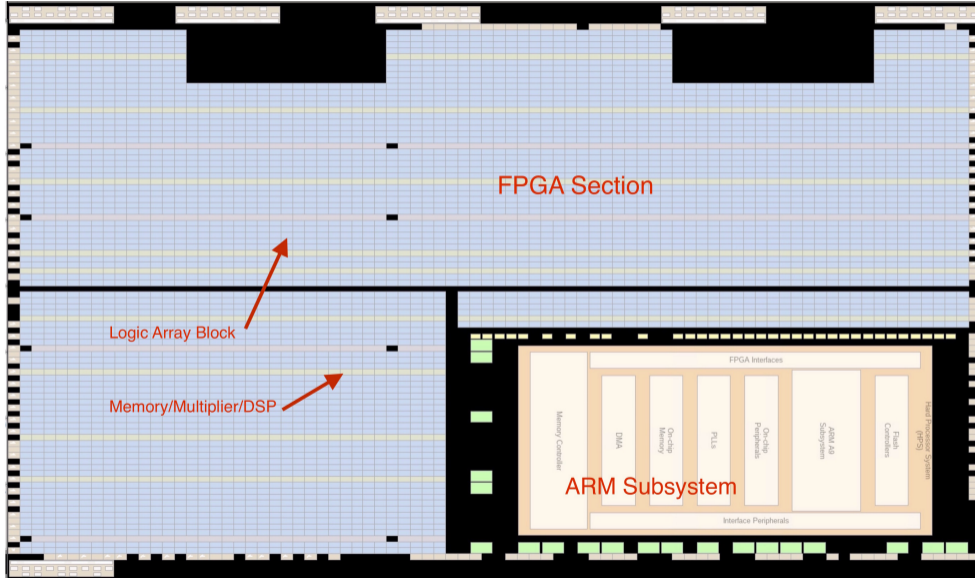
[Cyclone V - more](#)

[Cyclone V HPS](#)

[Cyclone V FPGA](#)

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Intel Cyclone V Chip Floorplan



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Altera DE1 SoC Board

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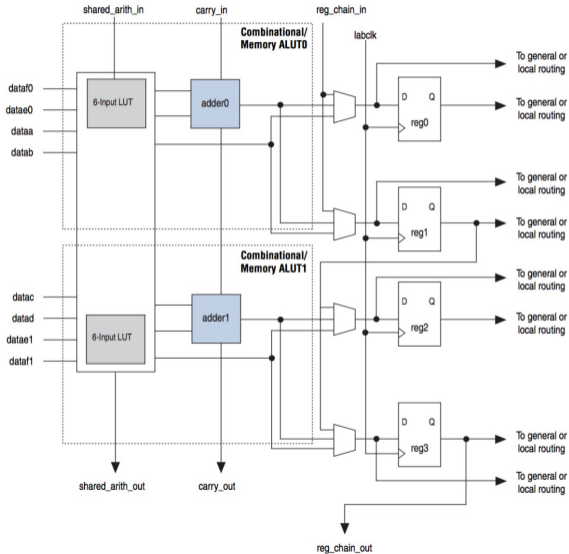
Cyclone V HPS

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Intel Cyclone V - FPGA - Advanced Logic Module - Overview

Figure 1-5. High-Level Block Diagram of the Cyclone V ALM



Overview

Atera DE1 SoC Board

Cyclone V

Atera DE1 board

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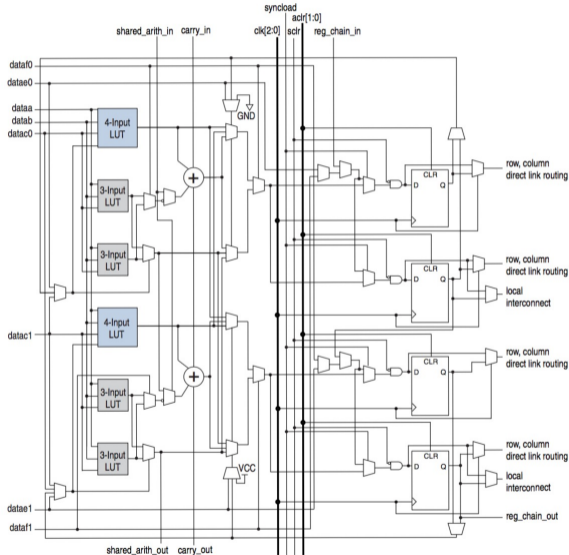
Cyclone V HPS

Cyclone V FPGA

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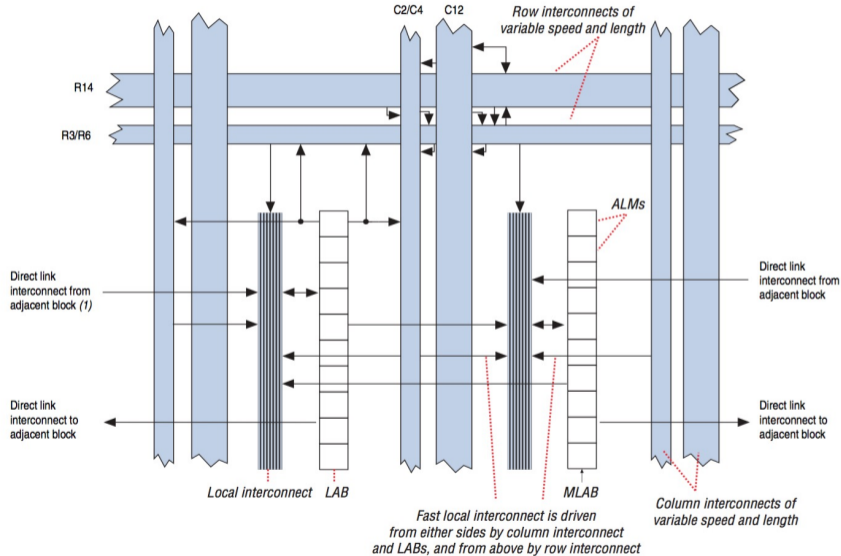
Intel Cyclone V SE - Advanced Logic Module - Detail

Figure 1-6. ALM Connection Details for Cyclone V Devices



Intel Cyclone V SE - Logic Array Block Routing

Figure 1-1. LAB Structure and Interconnects Overview in Cyclone V Devices



Intel Cyclone V SE - Resources

Resource		Member Code			
		A2	A4	A5	A6
Logic Elements (LE) (K)		25	40	85	110
ALM		9,434	15,094	32,075	41,509
Register		37,736	60,376	128,300	166,036
Memory (Kb)	M10K	1,400	2,700	3,970	5,570
	MLAB	138	231	480	621
Variable-precision DSP Block		36	84	87	112
18 x 18 Multiplier		72	168	174	224
FPGA PLL		5	5	6	6
HPS PLL		3	3	3	3
FPGA GPIO		145	145	288	288
HPS I/O		181	181	181	181
LVDS	Transmitter	32	32	72	72
	Receiver	37	37	72	72
FPGA Hard Memory Controller		1	1	1	1
HPS Hard Memory Controller		1	1	1	1
ARM Cortex-A9 MPCore Processor		Single- or dual-core	Single- or dual-core	Single- or dual-core	Single- or dual-core

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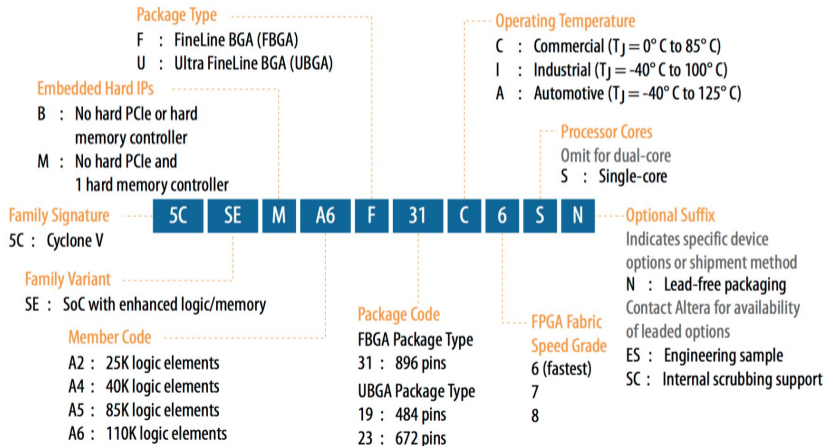
[Cyclone V FPGA](#)

[VLSI - Standard Cell Design](#)

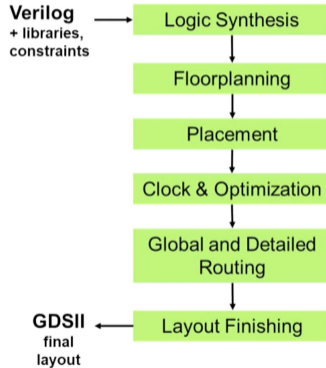
Intel Cyclone V 5CSEMA5F31C6N

Figure 4: Sample Ordering Code and Available Options for Cyclone V SE Devices

The SEU internal scrubbing feature is available for Cyclone V E, GX, SE, and SX devices with the "SC" suffix in the part number. For device availability and ordering, contact your local Altera sales representatives.



OpenROAD: Usage



- **SKY130:** 350+ tapeouts on Google-SkyWater, Efabless chipignite shuttle
- **GF12:** Mixed-signal SOC tapeout
- **Intel22/16:** Army Research Labs projects
- **Now supporting:** GF12, GF55, GF180, Intel22/16, TSMC65, SKY90, SKY130 and more



VLSI Design - OpenROAD

<https://youtu.be/DuqdMc4Kc3k>

Secure bus (bus.ucsd.edu:54 (miberty)) - VNC Viewer

Applications | omars@pc-3.ucsd.edu | OpenROAD | Terminal - @02277150b... | 1 2 3 4 5 6 7 8 9 10 | Sun 2 Apr, 14:04 | miberty

File View Tools Windows Options Help

Fit Find Inspect Timing P/G Insts Reset Clocks Sel IO

Display Control

- via8
- metal9
- via9
- metal10
- Nets
- Signal
- Power
- Ground
- Clock
- Instances
- StdCells
- Buffers/n...
- Combinati...
- Sequential
- Clock tree
- Level shifter
- Macro
- Pads
- Physical
- Fill cell
- Endcap
- Whitcap
- Tie high/low
- Antenna
- Cover
- Bump
- Other
- Blockages
- Rules
- Rows
- Inspector
- Tracks

Scripting

```
... select -name "max cap" -type Inst -highlight 3
... select -name "max length" -type Inst -highlight 3
... select -name "wire" -type Inst -highlight 3
... select -name "rebuffer" -type Inst -highlight 4 ;# red
... select -name "split" -type Inst -highlight 5 ;# dark green
...
```

Inspector TEL commands

Hierarchy Browser

Instance	Master	Instances	Macros	Modules	Area
<top>	swerv_wrapper	4,200/89,273	0/28	2/25	208
mem	mem	0/2,169	0/28	2/11	11
swerv	swerv	5,881/82,904	0/0	4/12	182
dec	dec	3,493/24,803	0/0	3/3	59
exu	exu	14,585/14,...	0/0	0/0	34
ifu	ifu	3,490/11,473	0/0	2/2	23
isu	isu	4,825/26,062	0/0	2/3	53
Leaf insta...		5,881	0	0	12
Leaf instances		4,200	0	0	14
Physical only		229,571	0	0	890

Inspector Hierarchy Browser

Source: OpenROAD

MEng VLSI - FPGA
Introduction

Prof. Dr.-Ing.
Friedrich Beckmann

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Altera DE1 SoC Board

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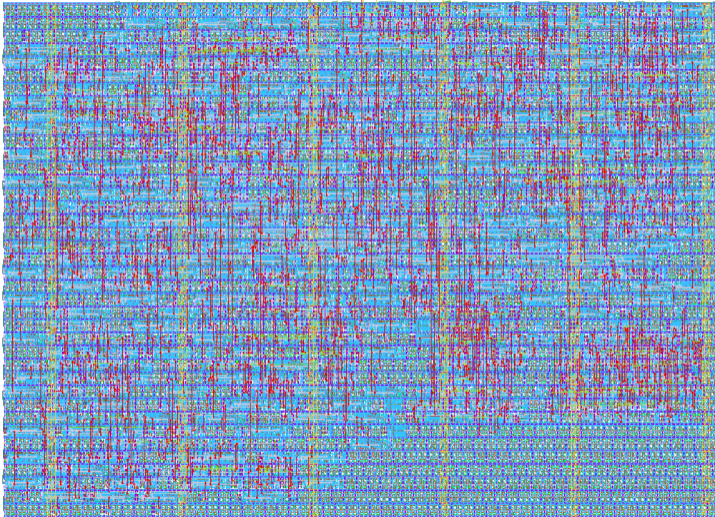
Cyclone V HPS

Cyclone V FPGA

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Design

VLSI Design - Chip Layout View - Tintytapeout - VGA Clock

https://tinytapeout.com/chips/ttihp0p2/tt_um_vga_clock



Source: TinyTapeout

Overview

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