

MEng VLSI Module - Overview

Prof. Dr.-Ing. Friedrich Beckmann

Hochschule Augsburg

► Schedule

- Lectures (Färber, Beckmann) 10 weeks until 21st of May
- Lecture: E4.02 / FPGA Lab E6.04
- Moodle: Information and Assignments
- Ulster Students: Miniprojects - typically one week full time effort
- Ulster Students: VLSI/COM: Combined Miniprojects, two weeks effort
- Exam 120 Minutes (70%) and Miniproject report + presentation (30%) ⇒ Final Grade

► Hans Färber - Essentials of VHDL

- Design Collaboration Using Distributed Version Management
- FPGA Toolchain in a Virtual Machine Environment
- VHDL Language Fundamentals
- VHDL Modelling Concepts for Combinational and Synchronous Building Blocks
- Introduction to Finite State Machines
- Prototype Testing on FPGA Prototype Boards
- Documentation and Presentation

► Dr. Friedrich Beckmann - VLSI Designflow

- FPGA Introduction
- Standard Cell Design for Digital Circuits
- Placement and Routing
- OpenROAD Designflow RTL to GDSII
- Static Timing Analysis

- ▶ Moodle online platform
 - ▶ Information and Assignments
 - ▶ Forum for questions
- ▶ Git
 - ▶ Version Control System
 - ▶ <https://gitlab.elektrotechnik.hs-augsburg.de/haf/2026-vlsi-fpga-flow-lab>
 - ▶ Team Repositories for Assignments
- ▶ Altera DE1 Boards / Lab at Home
 - ▶ All students are expected to have a working CAD environment on the laptop
 - ▶ **Virtual Machine with CAD Software**
 - ▶ Preconfigured Virtual Machine (Virtualbox) by Hans or
 - ▶ Build your own inside a Virtual Machine (Debian/Ubuntu)
 - ▶ Install the Software on your native Linux system