Technische
Hochschule
Augsburg

VLSI Design Module

Toolchain and Language Introduction

J Färber

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Contents

Tools and Language Introduction

Learning Objectives

After completing this unit, you will be able to:

- Navigate and understand the VHDL project directory structure
- Run the toolchain (GHDL, GtkWave, Quartus) using Makefiles
- Simulate a first VHDL design and download it to the FPGA board

Design Flow in VLSI Design

FPGA Design Flow

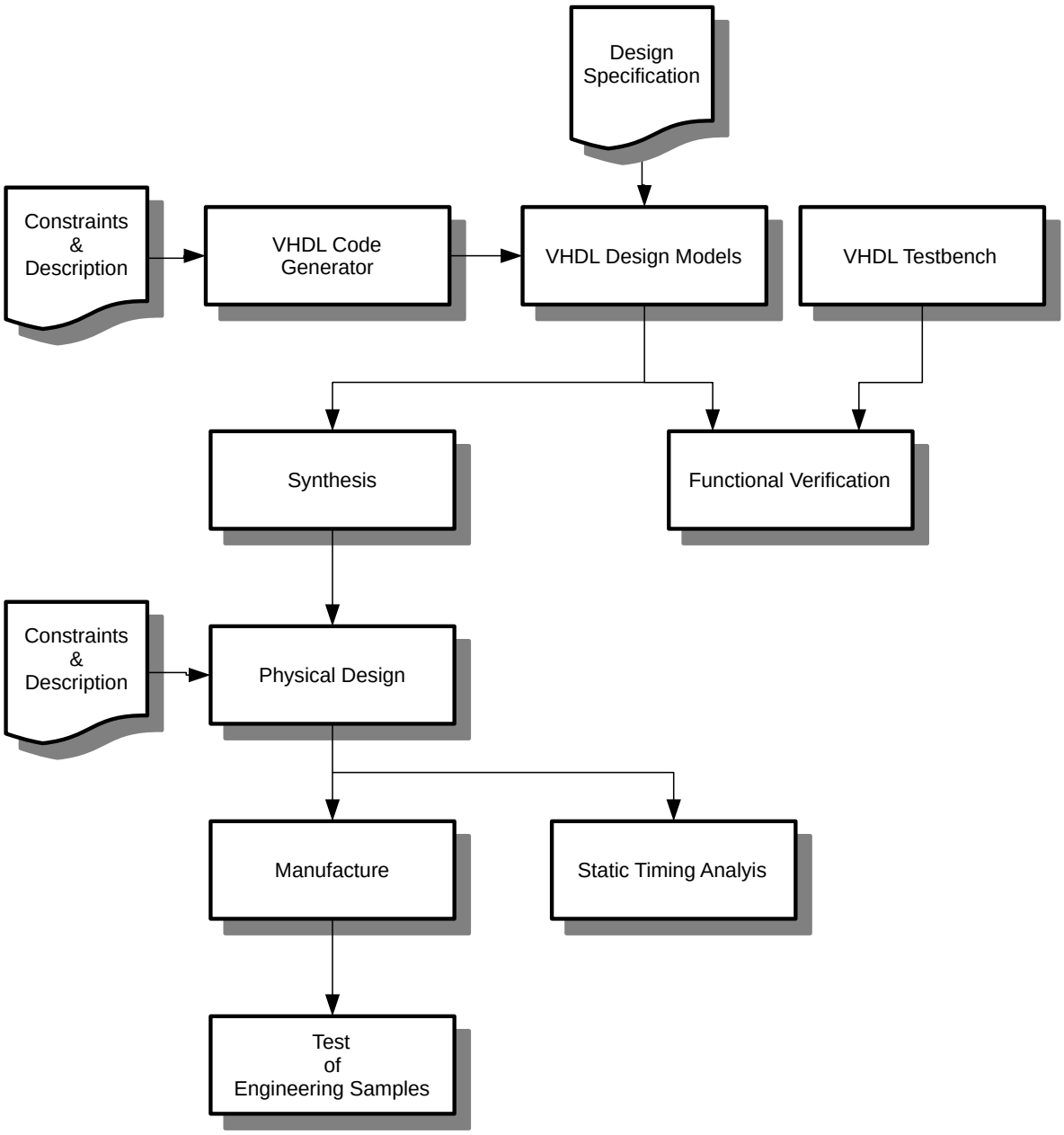

Figure 1: FPGA Design Flow

Design Flow - Simplified

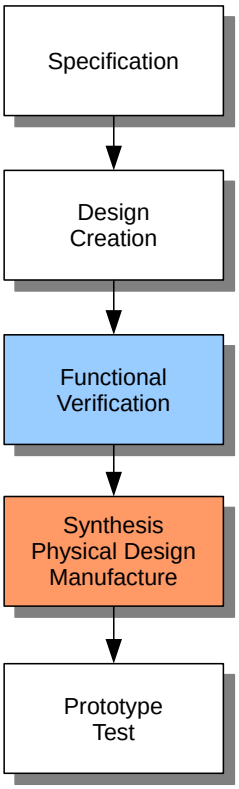

Figure 2: Simplified Design Flow

Design Flow - Simulation

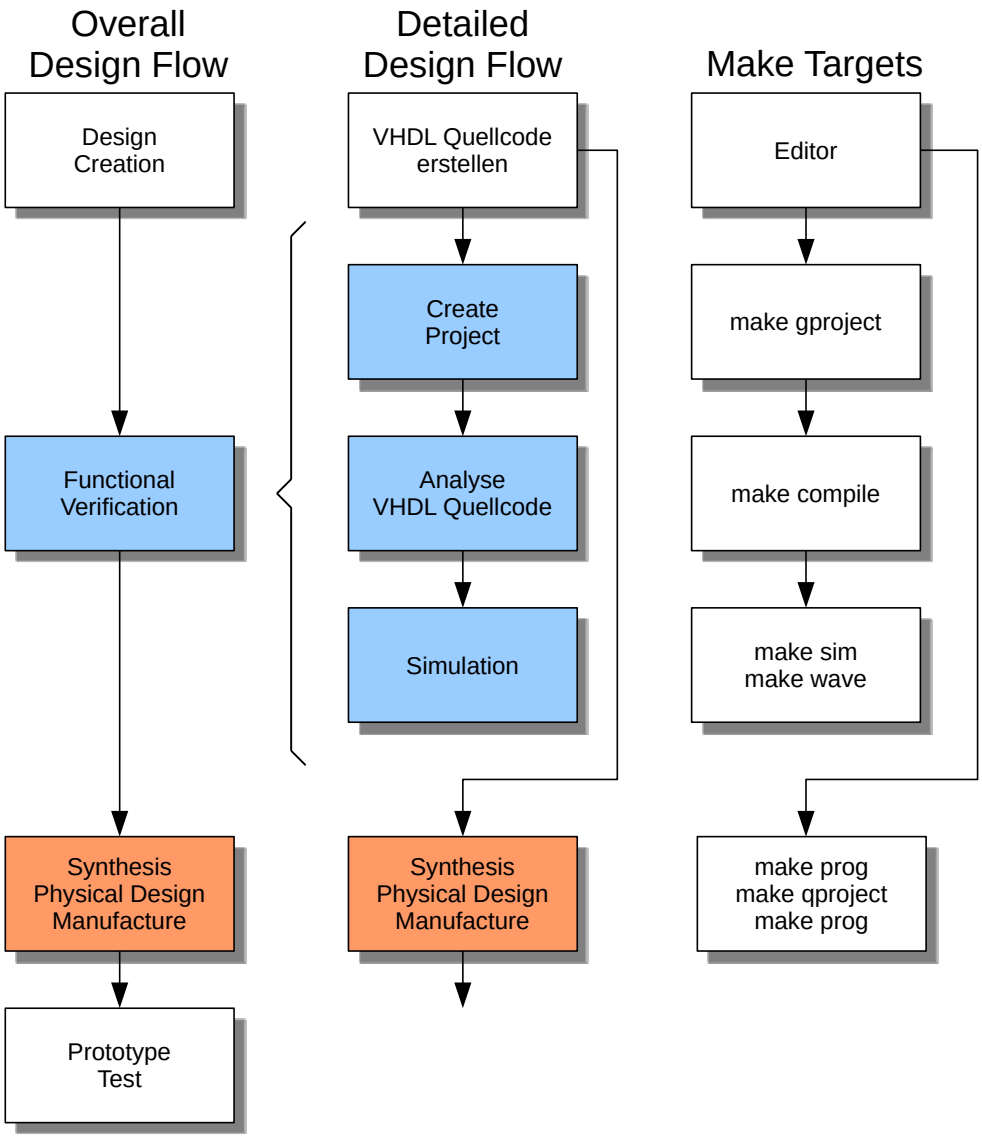

Figure 3: Simulation using makefile

Design Flow - Place & Route

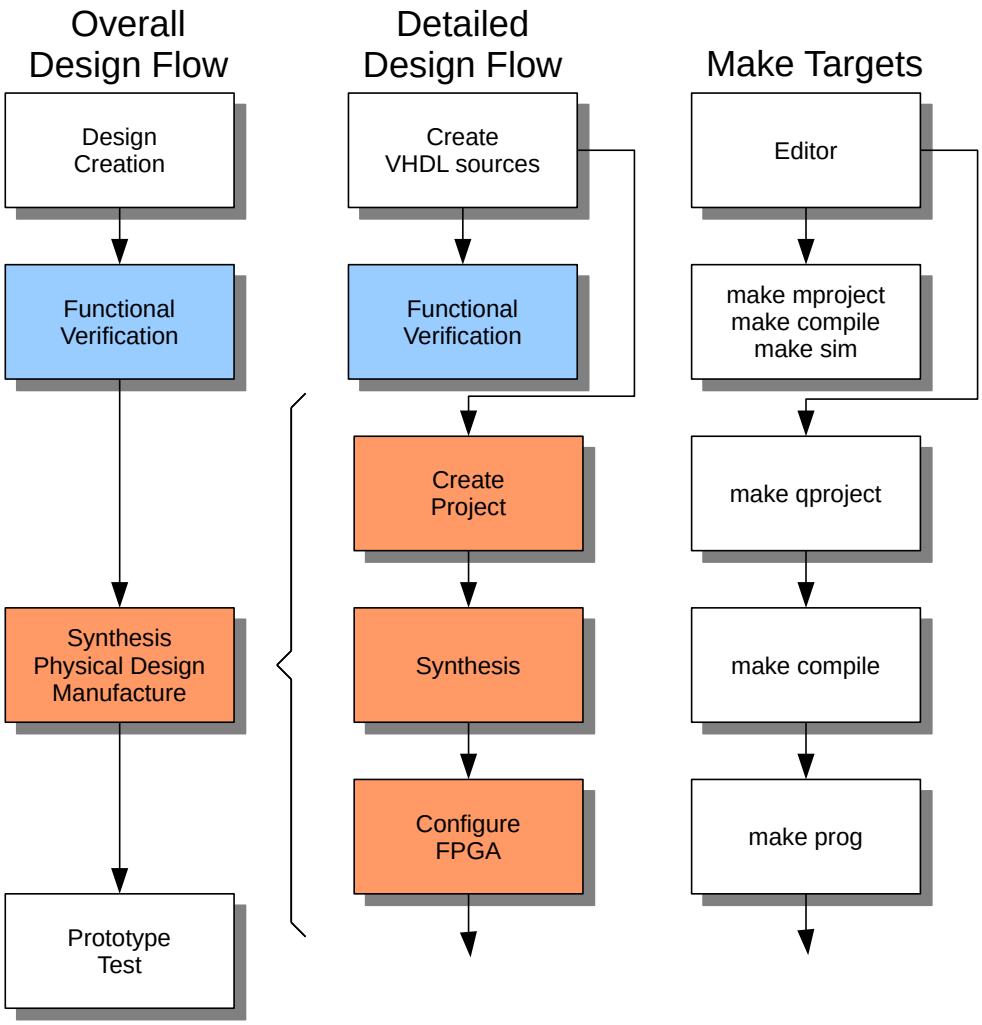

Figure 4: Place & Route using makefile

A First VHDL Example -

[Mea25] Mealy, B., Tappero, F.: Free Range VHDL

Referring to [Mea25], chap. 2 VHDL Invariants

Schematic Symbol

Referring to [Mea25], chap. 3.1 .. 3.3 Library, Entity, Architecture

Truth Table

b	a	y
0	0	
0	1	
1	0	
1	1	

Boolean Equation

y =

Timing Diagram

VHDL Testbench

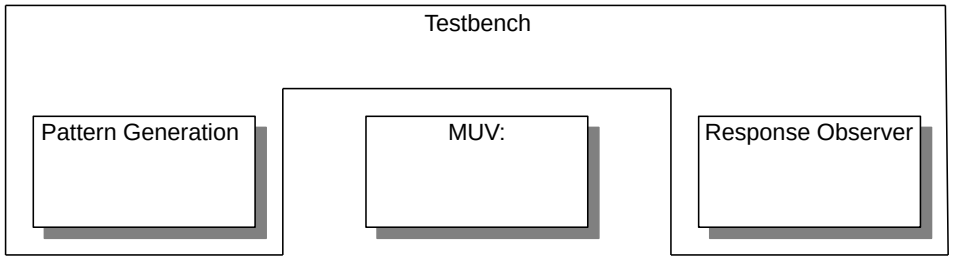

Figure 5: VHDL Testbench - General Structure

Module Hierarchy

ENTITY(ARCHITECTURE)

```
t_and2gate(tbench)
  and2gate(equation)
```

Filenames

```
vlsi-fpga-lab-20xx_lastname_firstname
|
+---src
|       and2gate_equation.vhd
|       t_and2gate.vhd
|
+---sim
|   |   makefile
|   |
|   +---and2gate
|   |       makefile
|   |
```

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY t_and2gate IS
END t_and2gate;

-------------------------------------------------------------------------------

ARCHITECTURE tbench OF t_and2gate IS

  COMPONENT and2gate IS
    PORT (
      a_i : IN  std_ulogic;
      b_i : IN  std_ulogic;
      y_o : OUT std_ulogic);
  END COMPONENT and2gate;

  -- definition of a clock period
  CONSTANT period : time := 10 ns;

  -- component ports
  SIGNAL a_i : std_ulogic;
  SIGNAL b_i : std_ulogic;
  SIGNAL y_o : std_ulogic;

BEGIN  -- tbench

  -- component instantiation
  MUV : and2gate
    PORT MAP (
      a_i => a_i,
      b_i => b_i,
      y_o => y_o);

  stimuli_p : PROCESS

  BEGIN
    a_i <= '0';                         -- set a value to input a_i
    b_i <= '0';                         -- set a value to input b_i
    WAIT FOR period;                    -- values are assigned here

    a_i <= '1';                         -- change value of a_i
    WAIT FOR period;









    WAIT;
  END PROCESS;

END tbench;
```

Prototype Testing

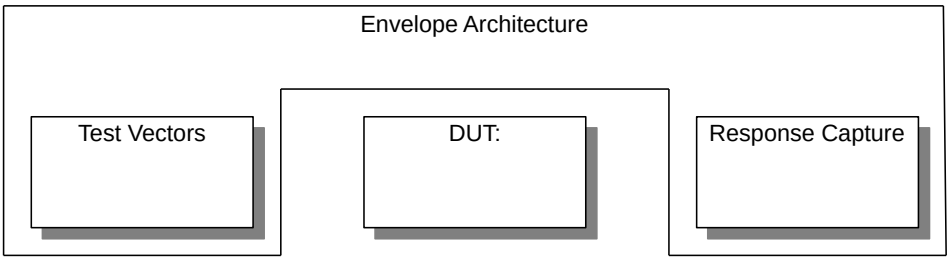

Figure 6: Envelope Architecture for Prototype Testing - General Structure

Module Hierarchy

ENTITY(ARCHITECTURE)

```
de1_and2gate(structure)
  and2gate(equation)
```

Filenames

```
vlsi-fpga-lab-20xx_lastname_firstname
|
+---src
|       and2gate_equation.vhd
|       t_and2gate.vhd
|       de1_and2gate_structure.vhd
|
+---sim
|   |   makefile
|   |
|   +---and2gate
|   |       makefile
|   |
+---pnr
|   |   makefile
|   |
|   +---de1_and2gate
|   |       de1_and2gate_pins.tcl
|   |       makefile
|   |
```

```
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;

--------------------------------------------------------------------------------

ENTITY de1_and2gate IS
  PORT (
    SW   : IN  std_ulogic_vector(1 DOWNTO 0);  -- Toggle Switch[2:0]
    LEDR : OUT std_ulogic_vector(2 DOWNTO 0)   -- LED Red[2:0]
    );
END de1_and2gate;

--------------------------------------------------------------------------------

ARCHITECTURE structure OF de1_and2gate IS

  COMPONENT and2gate IS
    PORT (
      a_i : IN  std_ulogic;
      b_i : IN  std_ulogic;
      y_o : OUT std_ulogic);
  END COMPONENT and2gate;

BEGIN

  -- assigning input signals to LEDs
  LEDR(0) <= SW(0);
  LEDR(1) <= SW(1);

  -- connecting device under test with peripheral elements
  DUT : and2gate
    PORT MAP (
      a_i => SW(0),
      b_i => SW(1),
      y_o => LEDR(2));

END structure;
```

Further Reading: [Mea25], chap. 4.1 .. 4.5 Concurrent Statements

Design Project Directory Structure

```
vlsi-fpga-lab-20xx_lastname_firstname
|
|-- ReadMe.md
|
+---src
|       and2gate_equations.vhd
|       t_and2gate.vhd
|       de1_and2gate_structure.vhd
|
+---sim
|   |   makefile
|   |
|   +---and2gate
|   |   |-- makefile
|   |   |-- makefile.sources
|   |   `-- view_signals.gtkw
|   |
|   +---or2gate
|   |   |-- makefile
|   |   |-- makefile.sources
|   |   `-- view_signals.gtkw
|   |
+---pnr
|   |   makefile
|   |
|   +---de1_and2gate
|   |       de1_and2gate_pins.tcl
|   |       makefile
|   |
|   +---de1_or2gate
|   |       de1_or2gate_pins.tcl
|   |       makefile
|   |
|
+---scripts
|       de1_pin_assignments_minimumio.tcl
|
...
```

Makefile Hierarchy

```
vlsi-design-lab
|
+-- src/
|   |-- e_
|   |-- and2gate_equation.vhd
|   |-- t_and2gate.vhd
|   \-- de1_and2gate_structure.vhd
|
+-- sim/
|   |-- makefile
|   |
|   |-- and2gate/
|   |   |   +-------------------------------------+
|   |   |-- |makefile                             |
|   |   |   +-------------------------------------+
|   |   |   |PROJECT = and2gate                   |
|   |   |   |include ./makefile.sources           |
|   |   |   |SOURCE_FILES = $(SYN_SOURCE_FILES) \ |
|   |   |   |../../src/t_$(PROJECT).vhd           |
|   |   |   |include ../makefile                  |
|   |   |   +-------------------------------------+
|   |   |
|   |   |   +-------------------------------------+
|   |   \-- |makefile.sources                     |
|   |       +-------------------------------------+
|   |       |SYN_SOURCE_FILES = \                  |
|   |       |../../src/and2gate_equation.vhd \    |
|   |       |                                     |
|   |       +-------------------------------------+
|
|
+-- pnr/
|   |-- makefile
|   |
|   |-- de1_and2gate/
|   |       +-----------------------------------------------------+
|   |       |makefile                                             |
|   |       +-----------------------------------------------------+
|   |       ||SIM_PROJECT_NAME = and2gate                         |
|   |       |PROJECT = de1_$(SIM_PROJECT_NAME)                |
|   |       |...                                                  |
|   |       |include ../../sim/$(SIM_PROJECT_NAME)/makefile.sources|
|   |       |SOURCE_FILES = $(SYN_SOURCE_FILES) \                 |
|   |       |../../src/$(PROJECT)_structure.vhd                   |
|   |       |include ../makefile                                  |
|   |       +-----------------------------------------------------+
|   |   |
|   |   \-- de1_and2gate_pins.tcl
...
```

Summary

- FPGA Design Flow
- Design Project Directory Structure
- Flow Automation using makefile
- Design Hierarchy

Laboratory Exercise #0

Checklist - Preparatory Work

- ☐ Installation of Virtual Machine
- ☐ Download of design project directory
- ☐ Learn VSCodium IDE with Makefile (`make wave`, `make compile`, `make prog`)
- ☐ Understand Git basics (`git add`, `git commit`, `git tag`)
- ☐ Verify `and2gate` in simulation and on the FPGA board
- ☐ Circuit diagram of `de1_or2gate_structure.vhd`
- ☐ or2gate - Verification, Synthesis and prototype testing
- ☐ xor4 - Verification, Synthesis and prototype testing
- ☐ Circuit diagram of `xor4_equation.vhd`
- ☐ mux2to1 - Verification, Synthesis and prototype testing
- ☐ Git commit and tag: `lab#0_setup`
- ☐ Push to remote repository

Checklist - Laboratory Work

- ☐ Discuss your models and circuit diagrams with your laboratory supervisors
- ☐ Check in your results in your Git repository and tag it with `lab#0_setup`